IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Zhiqing Li et al.	Examiner: Pizarro Crespo, Marcos D
Serial No.: 10/729,859	Attorney Docket: NAY 0001 PA/31558.2
Filed: December 5, 2003	Confirmation No.: 8497
For: MAGNETIC FIELD EFFECT TRANSISTOR, LATCH AND METHOD	

Commissioner for Patents
Alexandria, VA 22313-1450
U.S.A.

DECLARATION PURSUANT TO 37 CFR 1.132

1. I, Zhiqing Li, am a named inventor in the above-noted application.

2. I have carefully reviewed the application and the pending claims with my co-inventors.

3. After review, we have concluded that co-inventor Ping Shum has only contributed to the subject matter in claims 12 to 14 of the application.

4. I am also a co-author of two papers entitled, respectively: "A CMOS Magnetic Latch with Extremely High Resolution" ("Paper I"), and "Weak Magnetic Field Pattern Detection by CMOS Magnetic Latch" ("Paper II"). Paper I was first published on December 8, 2002 in the *2002 International Electron Devices Meeting Technical Digest* ("2002 IEDM"), and Paper II was first published in 2003. Copies of each paper and the cover pages of the 2002 IEDM are attached as Appendix A.

5. Each of Paper I and Paper II names Z.Q. Li and X.W. Sun as authors. Z.Q. Li is the same person as Zhiqing Li and X.W. Sun is the same person as Xiaowei Sun, both being co-inventors in this application.

6. Co-inventor Ping Shum contributed to the concepts disclosed at the following portions of the papers: the 3rd paragraph of the Section "Principle", the Section "Conclusion", and Fig. 2 of Paper I; and the 2nd paragraph of the Section "Introduction", the 4th paragraph of the Section "Results and Discussion", and Figs. 1 and 3(a) of Paper II. However, as these concepts were not the focus of each of the papers, Ping Shum was not named as an author in the papers.

7. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that wilful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such wilful false statements may jeopardize the validity of the application or any patent issued thereon.

Declared in **Singapore,** this day of April 21, 2006

By _____
Zhiqing Li

Appendix A to Declaration by inventor Li

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A CMOS Magnetic Latch with Extremely High Resolution

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Abstract

A novel CMOS magnetic latch with extremely high magnetic resolution based on a single split-drain magnetic field-effect transistor is reported. The minimum detectable magnetic flux density is less than 4 μT. The resolution for magnetic pattern recognition is less than 2 mT. The breakthrough has been achieved by importing a positive feedback.

Introduction

The magnetic field-effect transistor (MAGFET) is a kind of magnetic field sensor that is fully compatible with standard CMOS process and whose magnetic sensitivity is linearly dependent on the magnetic flux density applied perpendicularly to the device surface. It is often combined together with other integrated electronic circuits to detect the strength of the applied magnetic field[1][2][3] or to realize a magnetic field-related function[4][5][6]. In some cases, it is also utilized to recognize a magnetic field pattern[7][8]. Unfortunately, the magnetic sensitivity of the MAGFET is intrinsically low. Its magnetic resolution is limited very much. Although the MAGFET array has been introduced to improve the magnetic sensitivity[3][5][7][8], the area occupied by the sensor array was greatly increased, and the spatial resolution was decreased accordingly, while the improvement in the magnetic resolution was not significant.

The multi-gate technique has also been employed to increase the magnetic sensitivity of the MAGFET[9]. In that case, a longitudinal electric field was established in the channel by the longitudinal multigates, and the carrier velocity was increased and thus the Lorentz deflection of carriers was enhanced by the longitudinal electric field. With good linearity, this longitudinally multigate-structured MAGFET is good for linear applications, although its bias condition is stringent in order to overcome the pre-existed longitudinal carrier velocity saturation. In fact, the linearity in magnetic sensitivity is not required in magnetic pattern recognition. For nonlinear applications, it should be more efficient to directly develop a lateral electric field in the MAGFET channel to deflect the carriers. Based on this idea, we hereby present a novel CMOS magnetic sensor for nonlinear applications. We call the sensor a magnetic latch, because the function of the device is exactly the same as an electric latch – the output of the device always latches to either one of the two stable states. The only difference between this magnetic latch and its electric counterpart is that the input signal for the magnetic latch is magnetic field strength, while the input for the electric latch is of electric nature. The proposed magnetic latch consists of only a single conventional MAGFET and a pair of laterally positioned floating gates. An extremely high magnetic resolution has been achieved with this magnetic latch. It is highly sensitive to magnetic field pattern and especially suitable for nonlinear applications.

Principle

Instead of replacing the normal gate of the MAGFET with a series of longitudinal ones as in [9], we propose to retain the original MAGFET, but add a pair of floating gates, which are located symmetrically along and on the two sides of the source-to-drain path of the MAGFET. The device layout of an n-channel magnetic latch and its suggested circuit schematic symbol are shown in Figs. 1(a) and 1(b), respectively, where inside of the dashed line frame in Fig. 1(a) is the conventional n-channel MAGFET, D1, D2, G and S stand for the two drains, gate and source of the MAGFET, respectively, and FG1 and FG2 are the corresponding acronyms of floating gate 1 and floating gate 2.

In the proposed magnetic latch, the two floating gates are made of the poly-silicon layer, which is other than and underlying the poly-silicon layer of the conventional MAGFET gate. The two floating gates are electrically isolated from but partially overlapping the normal MAGFET gate. When a voltage is applied across the two floating gates, two different potential levels will be developed in the inversion regions beneath the respective gates, a lateral potential gradient will be established across the inversion layer of the MAGFET, the carriers in the layer will be deflected, and finally the current imbalance will occur in between the two drains. Because there exists no other lateral electric field and the initial carrier velocity is zero, which is different from the situation in [9], the acceleration of this newly established lateral electric field on the deflection of the

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carriers should be much more significant than that of the longitudinal one in [9].

In order to associate the above lateral potential gradient to the applied magnetic field, we cross-connect the two drains to the two lateral floating gates. When the two drains are loaded with passive or active resistors or even its complementary p-channel counterpart, the current imbalance in the two drains caused by the applied magnetic field will be converted into voltage difference across the two drains. Because the two drains are cross-coupled with the two floating gates, a potential gradient will be built up in the inversion layer in such a way that the carriers in the layer are deflected further. The further deflection of the carriers will make the voltage difference across the two drains larger. This is a positive feedback process. It repeats until the voltage difference between the two drains reaches the positive or negative maximum levels allowed by the circuit configuration. As such, a latching function is realized, and a new magnetic field sensor, the CMOS magnetic latch, is invented. The configuration of the magnetic latch is shown in Fig. 2(a). For the convenience of combining it into circuits, its circuit schematic symbol is also given as in Fig. 2(b).

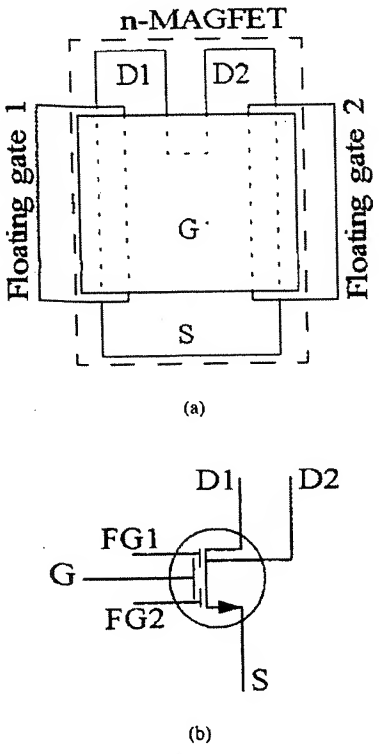

Fig. 1 The MAGFET with lateral floating gate pair. (a) Layout and (b) its suggested circuit schematic symbol

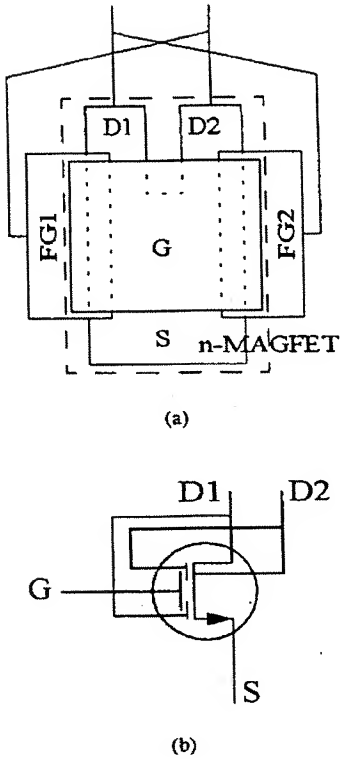

Fig. 2 The magnetic latch. (a) Layout and (b) its circuit schematic symbol

Experiment

The magnetic latch with the layout of Fig. 1(a) has been fabricated in a commercial 1.5 μm CMOS process. Its microphotograph is shown in Fig. 3. The conventional gate was made of poly2 layer, while the two floating gates are made of poly1 layer, *i.e.* the floating gates are beneath the normal gate. This arrangement allows better control of the lateral potential gradient in the channel along the two floating gates to deflect the carriers. When the two lateral floating gates of the latch are tied to the source, the sensor functions as a normal MAGFET. Under this configuration, the relative magnetic sensitivity was measured to be 3.8%/T with good linearity. This value is typical for a conventional n-channel MAGFET. The experimental dependency of the relative current imbalance in the two drains, $[(I_{d1}-I_{d2})/(I_{d1}+I_{d2})]\times 100\%$, on the applied magnetic flux density, B, is depicted in Fig. 4.

When this MAGFET with floating gate pair was configured as the magnetic latch as in Fig. 2 and loaded with two self-biased p-channel MOSFETs as shown in Fig. 5, its magnetic responses were measured by manually setting the DC magnetic flux density, B, step by step and by sweeping B up and down continuously. The experimental results are

shown in Figs. 6 and 7, respectively, without deducting the offset associated with V_o, where V_o is the output voltage of the magnetic latch with active load.

It can be seen from Fig. 7 that the output voltage presents a hysteretic dependency on the applied magnetic flux density, which is the intrinsic property of this magnetic latch. It is noted that the transitions of the output voltage are abrupt (less than 4 μT) when sweeping the magnetic field up and down, which implies an extremely high magnetic field resolution. The resolution of the magnetic latch for magnetic pattern detection, which is the width of the hysteretic loop in Fig. 7 or the transition region in Fig. 6, is less than 2 mT. These two resolutions, known to us, are the highest achieved ever by integrated Si magnetic field sensors in conjunction with other electronic circuits such as flip-flops for digital magnetic field detection. This highly sensitive magnetic latch based on only one MAGFET makes it a potential candidate for magnetic field pattern recognition with a high spatial resolution. Another feature of the hysteretic loop shown in Fig. 7 is that the closer to the transition point, the more noise the output voltage. It is worthy to point out that the hysteretic loop can be shaped by varying the load of the magnetic latch and/or the device geometry.

In conducting the measurement to obtain Fig. 7, the current driving the magnetic field generator and the gate voltage of the magnetic latch, V_G, were both supplied by the HP 4156 Semiconductor Parameter Analyser. The V_o was measured also by the HP analyser. The magnetic flux density, B, was calibrated by a Gaussmeter with an accuracy of 0.1 mT. The above magnetic resolution of less than 4 μT was derived out by calculating the proportionality of the current range occupied by the abrupt voltage transition region over the current required for generating 0.1 mT of B.

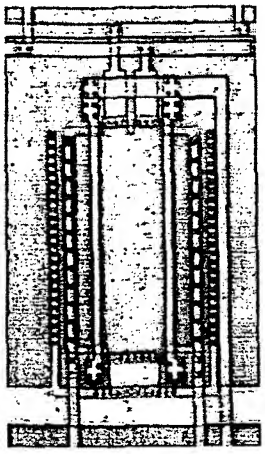

Fig. 3 Microphotograph of the fabricated CMOS magnetic latch

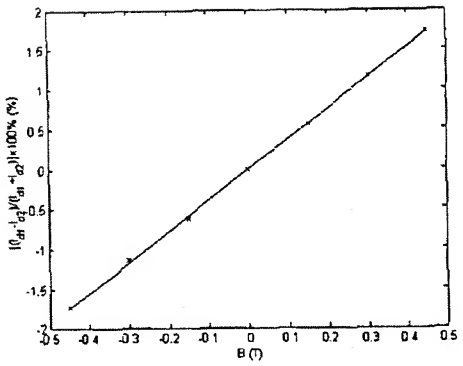

Fig. 4 Measured magnetic flux density-dependency of the relative current imbalance in the two drains of the sensor when the two lateral floating gates were tied to the source

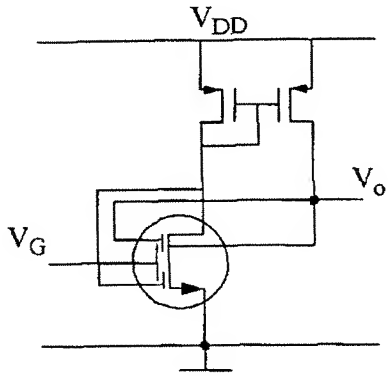

Fig. 5 Circuit setup of the magnetic latch for magnetic response measurement

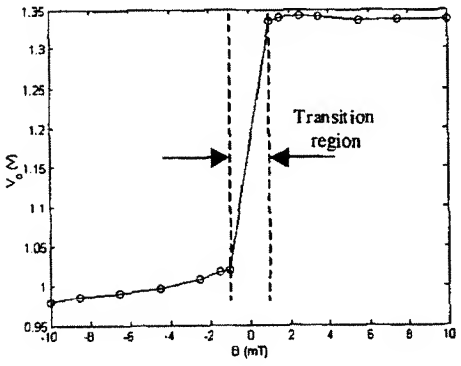

Fig. 6 Measured DC magnetic response of the magnetic latch when configured as in Fig. 5

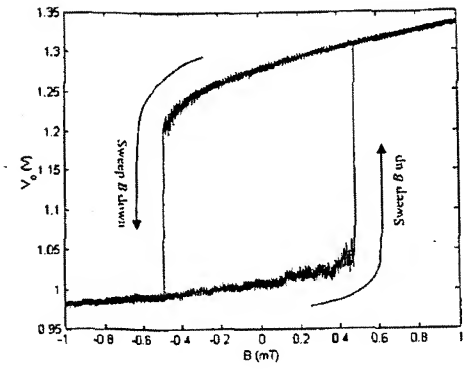

Fig. 7 Measured loop magnetic response of the magnetic latch when configured as in Fig. 5

Discussion

A. Effect of swapping the polysilicon layers for the floating gates and for the normal gate

Although the poly1 layer was used for the floating gates and the poly2 layer for the conventional one in our experiments, they can be swapped with each other. However, it can be expected that, under the latter configuration, the magnetic sensitivity of the magnetic latch will be degraded. This is because the thickness of the gate oxide of the poly2 layer is larger than that of the poly1 layer, and then a voltage at the poly2 floating gate will generate a weaker potential in the inversion layer than the same voltage at the poly1 floating gate.

B. Impact of process offset on the device performance

The offset always exists in all the CMOS process and is inevitable. It has significant impact on our magnetic latch, because this magnetic latch benefits from the positive feedback, and its magnetic performance can be best embodied only when no offset occurs in between the two drains. In the case that the offset appears and causes the magnetic latch latched up, a very strong DC magnetic field has to be exerted to fight against this latch-up and to balance the offset. The offset effect in a source-coupled differential MOSFET pair has been analyzed in detail[10]. It's well known that, when no magnetic field exists, a MAGFET can be modeled as a pair of common-source-common-gate MOSFETs[11][12]. Thus, the analysis of the offset effect in the common-source differential MOSFET pair can be directly applied to the MAGFET. Our experiments were carried out with offset avoided, although no offset cancellation circuitry was adopted. It was overcome by adjusting the gate voltage of the magnetic latch carefully. This is based on the fact that the offset of a MOSFET is gate voltage-dependent, and the offset in the two drains of a MAGFET can be cancelled when its gate voltage is at some critical value.

Conclusion

A new CMOS magnetic latch with the magnetic resolution of less than 4 μT and the magnetic pattern resolution of less than 2 mT has been designed, fabricated and tested. The breakthrough in magnetic resolution, together with its full CMOS-compatibility, makes this magnetic latch a promising candidate for nonlinear magnetic field detection. The magnetic hysteresis property also brings about the possibility of using this magnetic latch as a digital magnetic field memory.

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Weak Magnetic Field Pattern Detection by CMOS Magnetic Latch

Z. Q. Li, *Student Member, IEEE,* and X. W. Sun, *Member, IEEE*

***Abstract*—A CMOS magnetic latch for digital magnetic field detection is reported. It is based on a single split-drain magnetic field-effect transistor with a positive feedback imported by a pair of lateral floating gates. The magnetic latch achieves its maximum magnetic sensitivity when latch-up takes place. A linear equation is used to model the positive feedback and the latch-up process. By imposing a reset-evaluation mechanism, the magnetic latch is evaluated for digital magnetic pattern detection. Experimental results show that the minimum detectable magnetic flux density for the magnetic latch could be down to less than 0.1 mT with low bit error rate.**

***Index Terms*—CMOS magnetic latch, magnetic field-effect transistor (MAGFET), magnetic field measurement, magnetic pattern recognition.**

I. Introduction

DUE TO FULL CMOS process-compatibility and good magnetic linearity, the magnetic field-effect transistor (MAGFET) is often combined together with other integrated electronic circuits to detect the strength of the applied magnetic field [1], to realize a magneto-electric function [2], or to recognize a magnetic field pattern [3], [4]. Unfortunately, its magnetic resolution is limited by the intrinsically low magnetic sensitivity, and the bit error rate (BER) is high for weak digital magnetic field detection. The increment of oversampling rate could reduce the BER to some extent, but the frequency of the detectable magnetic field decreases accordingly. Although the MAGFET array has been introduced to improve the magnetic sensitivity [1], the area occupied by the sensor array was greatly increased, and the spatial resolution was decreased, while the improvement in the magnetic resolution was not significant.

In order to take full advantage of CMOS process-compatibility while achieving realistic usefulness, we have presented a new CMOS magnetic sensor—CMOS magnetic latch based on a single MAGFET [5]. The layout of the magnetic latch is redrawn in Fig. 1, where inside of the dashed line frame is the conventional n-channel MAGFET with two drains D1 and D2, gate G and source S. FG1 and FG2 are the two lateral floating gates that are inserted in between the gate G and the active layer of the conventional MAGFET and cross connected to D1 and D2. It has been shown that a high magnetic resolution could be achieved with this device, and it is exclusively suitable for digital magnetic field detection. In this paper, we shall report the latch-up condition of the CMOS magnetic latch, and show the experimental results of applying the magnetic latch to weak magnetic pattern recognition.

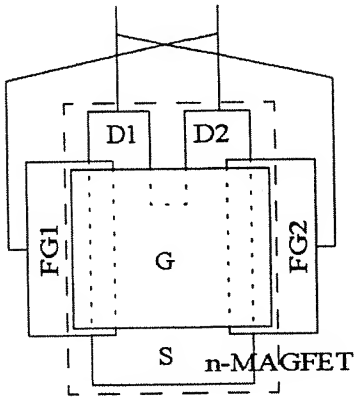

Fig. 1. Layout of the CMOS magnetic latch.

II. Principle

We have shown in [5] that the CMOS magnetic latch benefits from the positive feedback. The abrupt augment of the magnetic sensitivity occurs when the latchup takes place. In order to mathematically describe the positive feedback process, we firstly disconnect the two lateral floating gates, FG1 and FG2, from the two drains, D1 and D2, and bias the two floating gates at V_{FG1} and V_{FG2}, respectively. Assume, for simplicity, that the current imbalance in between the two drains, $I_{D1} - I_{D2}$, is linearly dependent on both the applied magnetic flux density, B, and the floating gate voltage difference, $V_{FG1} - V_{FG2}$; and the combined effect of B and $V_{FG1} - V_{FG2}$ on $I_{D1} - I_{D2}$ is additive to each other. We then have

$$I_{D1} - I_{D2} = k_B B + k_V (V_{FG1} - V_{FG2}) \tag{1}$$

where k_B and k_V are two coefficients describing the dependencies of $I_{D1} - I_{D2}$ on B and $V_{FG1} - V_{FG2}$, respectively.

When the two floating gates are cross-connected to the two drains to form a magnetic latch, and the two drains are loaded with respective resistors of the same resistance, R_D, (1) is modified to

$$I_{D1} - I_{D2} = k_B B/(1 - k_V R_D). \tag{2}$$

Equation (2) predicts that, theoretically, a very small magnetic flux density would cause the device to latch up if $R_D \geq 1/k_V$.

On one hand, the latch-up effect helps accomplish a high magnetic sensitivity. On the other hand, however, it may prevent the sensor from releasing under weak magnetic field. In

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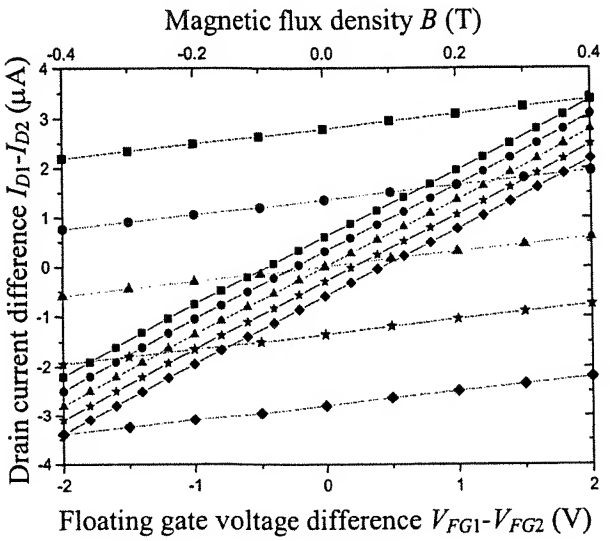

Fig. 2. Drain current imbalance dependencies on floating gate voltage difference, $V_{FG1} - V_{FG2}$, under various magnetic flux density, B, (solid lines referred to the bottom x-axis) and on B under various $V_{FG1} - V_{FG2}$ (dashed lines referred to the top x-axis). From top down, the solid lines correspond to $B = 0.4, 0.2, 0, -0.2, -0.4$ T, respectively, and the dashed lines correspond to $V_{FG1} - V_{FG2} = 2, 1, 0, -1, -2$ V, respectively.

order to circumvent this problem, a reset mechanism could be imposed, i.e., a transmission gate can be inserted in between the two drains of the latch. When the transmission gate is on, the two drains are short-circuited, and the latch is reset; when the transmission gate is off, the two drains are open-circuited, and the latch is in evaluation phase. This solution is also helpful for improving the magnetic resolution, because the device is now working in its unstable region during the reset phase, and a very weak disturbance from a magnetic field would cause the device to latch up in its evaluation phase.

III. Results and Discussion

The magnetic latch has been fabricated in a commercial 1.5 μm CMOS process. The conventional gate was made of poly2 layer, while the two floating gates are made of poly1 layer, i.e., the floating gates are beneath the normal gate. This arrangement allows better control of the lateral potential gradient in the channel along the two floating gates to deflect the carriers, so that a larger k_V can be achieved, and the latch-up may happen more easily. The threshold voltages of the poly1 and the poly2 transistors were measured to be 0.61 V and 0.89 V, respectively.

When the conventional gate was biased at 3 V, and the two drains both were biased at 4 V, the dependencies of the drain current imbalance, $I_{D1} - I_{D2}$, on the magnetic flux density, B, and the floating gate voltage difference, $V_{FG1} - V_{FG2}$, were tested, where the common-mode voltage of V_{FG1} and V_{FG2} was set to 4 V. The results are shown in Fig. 2. It can be seen from Fig. 2 that, within the region of consideration, $I_{D1} - I_{D2}$ is linearly dependent on B and $V_{FG1} - V_{FG2}$, and the contribution of B and $V_{FG1} - V_{FG2}$ to $I_{D1} - I_{D2}$ is additive to each other. The linear relationship holds only when both poly1 and poly2 transistors work in saturation region. Therefore, the assumptions for deriving (1) and (2) are reasonable. By conducting simple linear curve fitting in Fig. 2, we find $k_B = 1.50$ μA/T and

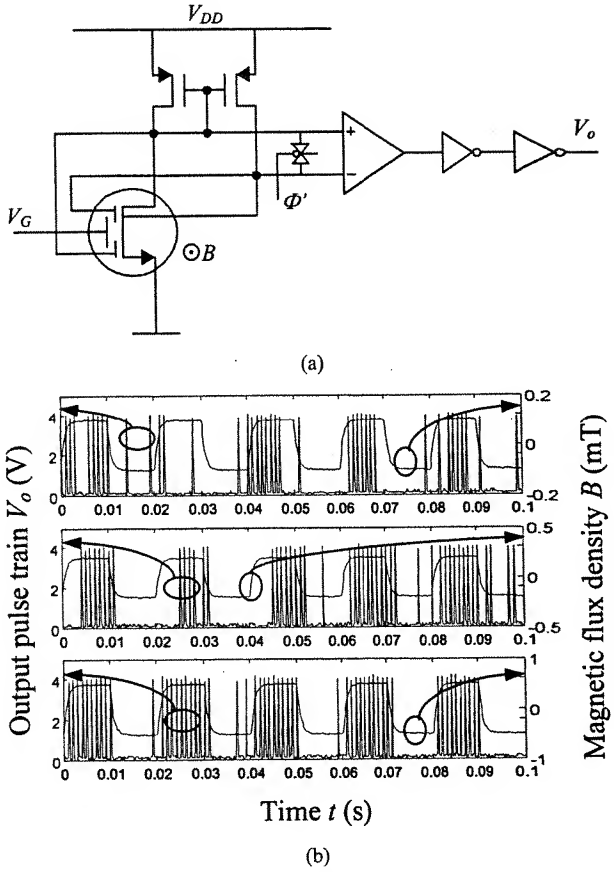

Fig. 3. Applying the CMOS magnetic latch to magnetic pattern detection. (a) Principle circuit schematic diagram. (b) Output pulse train of the detecting circuit and magnetic field pattern with amplitudes of 0.1, 0.2, and 0.5 mT.

$k_V = 1.38$ μA/V. These two factors are fabrication process-, device geometry- and bias-dependent. By applying the values of k_B and k_V to (2), the latch-up condition was calculated to be $R_D \geq 725$ kΩ under present biasing condition.

It has been shown in [5] that, when the latch was loaded with two self-biased p-channel MOSFETs, its magnetic response presented a hysteresis loop. This is the intrinsic property of latch-up. In that case, the small signal-equivalent output resistance of the active load is much larger than 1 MΩ, deep positive feedback was introduced, and latch-up was triggered easily.

To apply the magnetic latch to magnetic field pattern detection, a simple circuit was used. Fig. 3(a) shows the principle circuit schematic diagram. As discussed previously, a reset-evaluation mechanism is employed. The opamp works in open-loop mode functioning as a single-ended differential inverter. An air core coil is used to generate a linear magnetic field pattern.

A typical set of samples of the measured output pulse train V_0 and the applied magnetic field pattern B are shown and compared in Fig. 3(b) for $B = 0.1, 0.2$, and 0.5 mT. The clock frequency and oversampling rate here are set to 1 kHz and 10, respectively. By setting a proper decision criterion, the magnetic pattern could be easily extracted from the output pulse train. It's evident that, based on the magnetic latch, the magnetic field pattern resolution of down to 0.1 mT could be achieved with low BER under low oversampling rate; and by increasing oversampling rate, the magnetic pattern resolution could be further

increased to reach sub-Gauss range. Owing to the reset arrangement, the magnetic pattern resolution achieved here is higher than that predicted by the loop curve of the magnetic latch in [5].

IV. Conclusion

A CMOS magnetic latch has been designed, fabricated and applied to magnetic field pattern detection. The latch-up effect maximizes the magnetic sensitivity. By applying a simple linear model, the latch-up mechanism has been mathematical described, and the latch-up condition has been derived. A reset-evaluation mechanism was employed for weak magnetic pattern detection. By setting the transmission gate on and off alternatively, the magnetic latch operates in reset and evaluation phases accordingly. In conjunction with simple post-processing circuits, this magnetic latch has achieved a magnetic pattern resolution of 0.1 mT with low BER under low oversampling rate. The high magnetic resolution, together with its full CMOS process-compatibility, makes this magnetic latch a promising candidate for digital magnetic signal detection with low cost.

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